IN THE CLAIMS:
Please amend the claims, as follows:

1. (Currently amended) An input/output protection device for a semiconductor integrated circuit having a substrate of a first conduction type, an internal circuit, an input/output terminal, electrode wiring, and signal wiring, said protection device comprising:

a first region of a first diffusion layer fabricated in a region of the first conduction type of the semiconductor substrate, the first diffusion layer having a second conduction type opposite the first conduction type, said first region being connected to the input/output terminal;

a second region of said first diffusion layer of the second conduction type being held at a predetermined potential; and

a third region having a diffusion layer of the second conduction type fabricated at a bottom of the second region, the third region being connected to the second region of said first diffusion layer, said third region being fabricated at a location other than at a bottom of said first diffusion layer of said first region,

the first region being circularly enclosed by the second and third regions, said first region, said second region, and said third region thereby forming a parasitic bipolar transistor in which said first region serves as a collector thereof and said second region and said third region serve as an emitter thereof.

2. (Original Claim) An input/output protection device in accordance with claim 1, wherein the region of the first conduction type of the semiconductor substrate includes a fourth diffusion layer having an impurity concentration higher than that of the semiconductor

substrate.

3. (Original Claim) An input/output protection device in accordance with claim 2, wherein the impurity concentration of the fourth diffusion layer monotonously decreases in a direction from a surface of the semiconductor substrate to an inner section thereof.

4. (Original Claim) An input/output protection device in accordance with claim 2, wherein the third diffusion layer has a depth equal to or more than that of the fourth diffusion layer.

5. (Original Claim) An input/output protection device in accordance with claim 1, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

6. (Original Claim) An input/output protection device in accordance with claim 1, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

7. (Original Claim) An input/output protection device in accordance with claim 1, wherein the first and second diffusion layers are manufactured with a gate electrode disposed on a surface of the semiconductor substrate.

8. (Original Claim) An input/output protection device in accordance with claim 6, wherein the device separating isolation layer or the gate electrode is fabricated in a circular shape.

9. (Original Claim) An input/output protection device in accordance with claim 7, wherein the gate electrode is connected to the signal wiring of the internal circuit of the semiconductor integrated circuit.

10. (Original Claim) An input/output protection device in accordance with claim 7, wherein the gate electrode is fixed to a predetermined potential.

11. (Original Claim) An input/output protection device in accordance with claim 1, wherein:

the first conduction type is a p type and the second conduction type is an n type; and

the predetermined potential is a ground potential.

12. (Original Claim) An input/output protection device in accordance with claims 1, wherein:

the first conduction type is an n type and the second conduction type is a p type; and

the predetermined potential is a potential of a power source.

13. (Previously presented) An input/output protection device in accordance with claim 3 wherein the third diffusion layer has a depth equal to or more than that of th fourth diffusion layer.

14. (Previously presented) An input/output protection device in accordance with claim 2, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

15. (Previously presented) An input/output protection device in accordance with claim 3, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

16. (Previously presented) An input/output protection device in accordance with claim 4, wherein a lateral, bipolar transistor including the first diffusion layer as a collector, the second and third diffusion layers as an emitter, and the region of the first conduction type or the fourth diffusion layer as a base is put to operation.

17. (Currently amended) An input/output protection device in accordance with claim 2, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a ~~suffice~~ surface of the semiconductor substrate.

18. (Previously presented) An input/output protection device in accordance with claim 3, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

19. (Previously presented) An input/output protection device in accordance with claim 4, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

20. (Previously presented) An input/output protection device in accordance with claim 5, wherein the first and second diffusion layers are isolated from each other by a device separating isolation layer on a surface of the semiconductor substrate.

21-26. (Cancel)

27. (Previously presented) The protection device of claim 1, wherein a protection of said internal circuit occurs by an avalanche breakdown in which said first diffusion layer connected to said input/output terminal serves as a collector and said second and third diffusion layers serve as an emitter for a lateral bipolar transistor.